

DATA FLOW ORIENTED STORAGE

ABSTRACT OF THE DISCLOSURE

5 A Storage Reference Buffer (SRB) designed as an autonomous unit for all
Store operations that transfer data from the execution unit of a processor to the
memory hierarchy and Load operations that transfer of data from the memory
10 hierarchy to the execution unit of the processor. The SRB partitions up the Load and
Store operations into several smaller operations in order to perform them in parallel
with other Load and Store requests. System elements are included to determine
unambiguously which of these Load and Store operations may be performed without
waiting for prior operations to be completed. The SRB also includes system elements
15 to detect whether requests may be satisfied by existing entries in the SRB without
having to access the cache. The SRB is operated as a content addressable memory.
Load request are simultaneously launched to cache and to the SRB with the Cache
request being canceled if the Load request may be satisfied by an SRB entry.

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